

CLAIMS

What is claimed is:

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1. An integrated circuit, comprising:
    - 2 a set of voltage generators to generate a set of direct current (DC) voltages;
    - 4 a set of sense amplifiers coupled to compare a reference voltage with the set of DC voltages; and
    - 6 logic coupled to each sense amplifier in the set of sense amplifiers to interpret the comparison of the reference voltage and the set of DC voltages.
  - 1 2. The integrated circuit of claim 1 wherein the set of voltage generators is responsive to a set of configuration bits to determine the set of DC voltages.
  - 1 3. The integrated circuit of claim 2, further comprising a set of switches coupled between the set of voltage generators and the set of sense amplifiers to enable the set of DC voltages to be applied to the non-inverting input of each sense amplifier in the set of sense amplifiers.
  - 1 4. The integrated circuit of claim 2, wherein each voltage generator in the set of voltage generators is a digital-to-analog converter.
  - 1 5. The integrated circuit of claim 1, further comprising second logic coupled to open and close the set of switches to connect the set of DC voltages to the non-inverting inputs of the set of sense amplifiers.
  - 1 6. The integrated circuit of claim 5, wherein the second logic comprises a boundary-scan register.

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1 7. The integrated circuit of claim 5, wherein the second logic comprises an  
2 input/output loop back pattern generator.

1 8. A system, comprising:

2 an integrated circuit having a set of voltage generators to generate a set  
3 of direct current (DC) voltages, a set of sense amplifiers coupled to compare a  
4 reference voltage with the set of DC voltages, and logic coupled to each sense  
5 amplifier in the set of sense amplifiers to interpret the comparison of the reference  
6 voltage and the set of DC voltages; and

7 a structural tester coupled to the integrated circuit to apply a reference  
8 voltage to the inverting input of each sense amplifier in the set of sense amplifiers.

1 9. The system of claim 8, wherein the set of voltage generators is responsive to a  
2 set of configuration bits to determine the set of DC voltages.

1 10. The system of claim 8, wherein the integrated circuit further comprises a set of  
2 switches coupled between the set of voltage generators and the set of sense amplifiers  
3 to enable the set of DC voltages to be applied to the non-inverting input of each sense  
4 amplifier in the set of sense amplifiers.

1 11. The system of claim 8, wherein each voltage generator in the set of voltage  
2 generators is a digital-to-analog converter.

1 12. The system of claim 8, wherein the logic to interpret the comparison of the  
2 reference voltage and the set of analog voltages comprises a boundary scan register.

1 13. The system of claim 8, wherein the logic to interpret the comparison of the  
2 reference voltage and the set of analog voltages comprises input/output loop back  
3 compare circuitry

1    14. The system of claim 8, wherein the integrated circuit further comprises a set of  
2    switches coupled between the set of voltage generators and the set of sense amplifiers  
3    to enable the set of DC voltages to be applied to the non-inverting input of each sense  
4    amplifier in the set of sense amplifiers, and wherein the integrated circuit further  
5    comprises second logic coupled to open and close the set of switches.

1    15. The system of claim 14, wherein the second logic comprises a boundary-scan  
2    register.

1    16. The system of claim 14, wherein the second logic comprises an input/output  
2    loop back pattern generator.

1    17. A method of manufacturing an integrated circuit, comprising:  
2                coupling a set of levels generating circuits to a set of sense amplifiers,  
3    wherein the set of sense amplifiers are to compare a reference voltage to a set of direct  
4    current (DC) voltage levels generated by the set of levels generating circuits; and  
5                coupling the set of sense amplifiers to logic to interpret the comparison  
6    of the reference voltage and the set of voltage levels.

1    18. The method of claim 17, further comprising coupling the set of levels  
2    generating circuits to be responsive to a set of configuration bits to set the values of  
3    the set of DC voltage levels.

1    19. The method of claim 18, further comprising coupling a set of switches between  
2    the set of levels generating circuits and the set of sense amplifiers to enable the set of  
3    DC voltage levels to be applied to the non-inverting input of each sense amplifier.

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1 20. The method of claim 19, wherein coupling a set of levels generating circuits to  
2 a set of sense amplifiers comprises coupling a set of digital-to-analog converters to  
3 the set of sense amplifiers.

1 21. The method of claim 17, wherein coupling the set of sense amplifiers to logic  
2 to interpret the comparison of the reference voltage and the set of DC voltage levels  
3 comprises coupling the set of sense amplifiers to a boundary scan register to interpret  
4 the comparison of the reference voltage and the set of DC voltage levels.

1 22. The method of claim 17, wherein coupling the set of sense amplifiers to logic  
2 to interpret the comparison of the reference voltage and the set of DC voltage levels  
3 comprises coupling the set of sense amplifiers to input/output loop back compare  
4 circuitry to interpret the comparison of the reference voltage and the set of DC voltage  
5 levels.

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1 23. The method of claim 19, further comprising coupling second logic to open and  
2 close the set of switches.

1 24. The method of claim 23, wherein coupling second logic to open and close the  
2 set of switches comprises applying values from a boundary-scan register to open and  
3 close the set of switches.

1 25. The method of claim 23, wherein coupling second logic to open and close the  
2 set of switches comprises applying values from an input/output loop back pattern  
3 generator to open and close the set of switches, wherein the second logic comprises an  
4 input/output loop back pattern generator.

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1 26. An apparatus, comprising:  
2       an integrated circuit device having:  
3            a first number of input pins; and  
4            levels generating circuitry coupled to at least some of the first  
5            number of input pins, the levels generating circuitry being responsive to a set  
6            of configuration bits to enable concurrent input levels testing or parallel input  
7            levels testing of the first number of input pins using a second smaller number  
8            of input pins.

1 27. The apparatus of claim 26, wherein the levels generating circuitry comprises:  
2        a set of voltage generators to generate a set of direct current (DC)  
3        voltages;  
4        a set of sense amplifiers coupled to compare a reference voltage with  
5        the set of DC voltages; and  
6        logic coupled to each sense amplifier in the set of sense amplifiers to  
7       interpret the comparison of the reference voltage and the set of DC voltages.

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1 28. The apparatus of claim 27, further comprising a set of switches coupled  
2       between the set of voltage generators and the set of sense amplifiers to enable the set  
3       of DC voltages to be applied to the non-inverting input of each sense amplifier in the  
4       set of sense amplifiers.

1 29. The integrated circuit of claim 27, wherein each voltage generator in the set of  
2       voltage generators is a digital-to-analog converter.

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1 30. A method, comprising:

2 testing at least one integrated circuit device having a first number of

3 input pins and levels generating circuitry coupled to at least some of the first number

4 of input pins by:

5 receiving a set of configuration bits at the levels generating

6 circuitry; and

7 receiving test input levels at a second smaller number of input

8 pins to enable parallel input levels testing of the first number of input pins.

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1 31. The method of claim 30, further comprising:

2 generating direct current (DC) voltages;

3 comparing a reference voltage with the set of DC voltages; and

4 interpreting the comparison of the reference voltage and the set of DC

5 voltages.

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1 32. The method of claim 31, wherein receiving a set of configuration bits at a

2 levels generating circuitry comprises receiving a set of configuration bits at digital-to-

3 analog converters

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